Fast Protection of Strong Power Systems With Fault Current Limiters and PLL-Aided Fault Detection

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Abstract—In this paper, a new method is proposed that can be used to discriminate faults from switching transients. The method is primarily intended for use in systems where fast fault detection and fast fault clearing before the first peak of the fault current are required. An industrial system, in which high short-circuit power is desired but in which high short-circuit currents cannot be tolerated is an example of such a system. A phase-locked loop (PLL) is used to perform the discrimination. Computer simulations have been performed and it has been demonstrated that the output of the PLL is completely different for a fault compared to a switching transient. This difference can be used for discrimination between a fault and a switching transient.

Index Terms—Fault protection, phase-locked loop (PLL), power system, transients.

I. INTRODUCTION

HIGH SHORT-CIRCUIT power is often desired in an industrial system in order to connect and disconnect loads without causing disturbances to sensitive equipment or processes. With the high short-circuit power, a high fault current develops in case there are faults in the system. This high fault current has to be considered when designing the switchgear and other components that build up the power system. This is easily done in new installations but can be problematic when there is a need for higher short-circuit power in an existing system. In these cases, the installation of a fault current limiter could be an alternative to rebuilding the switchgear. The installation of a fault current limiter can also provide the opportunity to make connections in the power system that otherwise would not be possible due to fault currents that exceed the rating of the switchgear. One of these examples is the paralleling of two transformers. If a fault current limiter is installed as a sectionalizer between the two transformers, the system will experience the benefit of higher short-circuit power and in case of a fault in the system, the fault current limiter is operated and the system is sectionalized, thus reducing the fault current to levels which the system can handle. In [1], a trend toward increased short-circuit power is reported, which is also illustrated by an experience of more than 2 800 installations of fault-current limiters throughout the world.

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In this paper, the need for fast and reliable protection is discussed. Fault-current limiters are an essential building block in many systems as well as the need for fast and reliable fault detection. It is demonstrated that a phase-locked loop (PLL) can be used for power system protection purposes as an alternative to other methods. An investigation on how to use a PLL for the purpose of discriminating between a fault and a switching transient has been performed. Furthermore, the combination of protection relays and PLLs is discussed. It is proposed that the protection relay will detect the current transient and that the PLL will determine whether the current transient is caused by a fault or a switching transient. The protection relay and the PLL can consist of software implementations on a suitable hardware platform.

This paper is structured in the following way: First, a background on fault-current limiters and fault protection is given. This is followed by a description of the PLL and how the PLL can be used in a method to detect faults and discriminate between faults and switching transients. Then, a section with a case study is provided including computer simulations of the proposed method. Finally, there is a section with concluding remarks and proposal for future work. Furthermore, a short appendix describing some methods of estimating power system signals is added for convenience.

II. FAULT-CURRENT LIMITERS AND FAULT-CURRENT DIVERTERS

An apparent contradiction regarding the short-circuit power of a supply network is that whereas there are obvious advantages with a stronger network (less voltage dips, more and larger loads can be connected, less switching transients), there are also obvious disadvantages (high-fault currents in case of short-circuit faults in the system).

A. Fault-Current Limiters

One way of solving this contradiction is to use a fault-current limiter. A fault-current limiter is a device that during normal operating conditions allows a strong network but when a fault occurs, introduces enough impedance in the circuit so that the fault current is limited.

The purpose of a fault-current limiter is to limit the fault current so that its prospective peak value never is reached. The current limiting functionality can be achieved in several ways (e.g., current limiting reactors [2]; fuses [3]; triggered fuse [1]; superconductive fault–current limiters [4], [5]; and fuses [6] and power-electronic-based current limiters [7]–[10].

B. Fault-Current Diverters

Fault-current diverters can be used as an alternative to fault-current limiters. A current diverter consists of a switch that is in open position under normal operating conditions. When a fault is detected, the switch closes and short circuits the phases of the power system to earth at a predetermined location. This predetermined location is preferably chosen as close to the source as possible. The fault current will still flow from the source through the current diverter to earth and will continue to do so until the main circuit breaker (CB) clears the fault current. The benefit of a fault-current diverter is that the load that is connected to the system does not see the full short-circuit current once the switch has been closed. Thus, for the load, the fault-current diverter provides a limitation of the fault current. A current diverter is an easy solution to provide fault-current limiting functionality in a power network. The network downstream the current diverter experiences only a small residual current once the fault current has been commutated to the earth path.

One example of a current diverter is given in [11]. It is a device that in case of a short circuit involving an open arc operates quickly and achieves a short circuit between phases and earth, thus short-circuiting the arc. The voltage drop across the arc becomes practically zero, making the arc extinguish. Another example is given in [12], which is a similar device that uses the same principle.

One common feature of the described fault–current limiters and current diverters is that they must be able to operate within a few milliseconds after fault inception. The fault current must be limited before the first peak of the fault current. Taking into account that some of the fault-current limiters described before contain mechanical systems that require a certain time to operate, it can be concluded that fault detection is an essential prerequisite for a system containing a fault-current limiter. Some types of fault-current limiters do not depend on external fault detection—a superconductive fault-current limiter operates as soon as the superconducting properties of the device are changed due to the fault current and the fuse operates as soon as the current has increased above the fuse's designed operating current. For the other fault-current limiters, the fault detection has to be performed by external means.

III. POWER SYSTEM PROTECTION

As concluded in the previous section, power system protection is another important issue. It is essential for safe operation of the power system that faults are detected and cleared automatically in a fast and reliable manner so that the operation of the power system is not disturbed. A typical fault protection system is built from circuit breakers (CBs), protection relays, and primary transducers, such as voltage and current transformers and auxiliary equipment.

There are many methods and algorithms available to detect short-circuit current in a power system. One simple (but yet efficient) method is to estimate the current from measured current samples. If the magnitude of the estimated current is larger than a predetermined threshold it is assumed that a fault has occurred (magnitude relay). The estimation of the current can be performed using several different techniques, such as, for example,

by calculating the root mean square (rms) value as shown in the Appendix (A.1) by a fast Fourier transform (FFT) method as shown in the Appendix (A.2)–(A.4), or by a least-square (LSQ) method as shown in the Appendix (A.5)–(A.8). The accuracy of the estimation and the amount of information that is available for the estimation are correlated. In general, if more information is available, the estimation will become more accurate. On the other hand, if faster fault detection is required, the estimation becomes less accurate since less information is available. In an earlier paper, fast fault detection has been defined to be in the range of 1–2 ms after fault inception [13]. This short detection time is needed for the fault-current limiters as mentioned in the previous section. Some methods that have been suggested for use in transmission systems have the potential of being fast. These methods could be based on traveling waves [14], neural networks [15], wavelet transforms [16], and fault-generated noise [17].

Although it is sometimes possible to adapt the mentioned techniques for fast fault detection in power distribution systems, new techniques have been explored [18]. In the latter reference, a method for fast fault detection is described, which detects that a fault has occurred when five consecutive current samples are above a predefined threshold (i.e., the measured current samples are not fitted to a signal model). With proper signal processing (filtering), it was further demonstrated that it was possible to discriminate between a fault and common switching transients. In this paper, an alternative method to perform the discrimination is proposed.

Even though the detection of faults is the primary concern for fault protection devices (dependability), the ability to distinguish between a fault and a switching transient (security) is also important. Switching transients can, under certain circumstances, give rise to high currents, which are much larger in magnitude than normal load currents. In existing relay protection, capacitor energization and transformer energization have been detected by analyzing the measured current to find certain characteristics of the two types of current transients as described in, for example, [19]. A current transient caused by a transformer energization typically contains a superimposed dc component and a superimposed second harmonic component. A current transient caused by a capacitor energization typically contains higher frequency harmonic components. The harmonic components in the measured current can be identified with Fourier-based methods, but that typically requires more time. For fast fault detection purposes, other methods have to be investigated. The method that is proposed in this paper uses a PLL for that purpose.

IV. PROPOSED METHOD

In this section, the proposed method of using a PLL for discrimination between faults and switching transients will be described. First, a short description of the basics of a PLL is given. Second, a well-known implementation of a PLL suitable for simulation purposes is described and the relevant signals that are used for the actual discrimination between a fault and a switching transient are identified. Third, the tuning of the parameters of the PLL implementation is discussed and suggestions for a first selection of parameters is given.
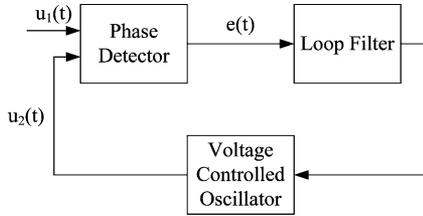
Fig. 1. Block diagram of a PLL.

A. Basics of a PLL

The PLL has been an important device in electronics and power system applications ever since the first implementation in the 1930s by de Bellescize, as mentioned in [20]. The first PLLs were analog devices but following the development in solid-state electronics and computer technology, the PLL has developed from an analog device via digital implementations to pure software implementations.

A PLL is a circuit that is used to synchronize an input signal with a reference signal (an output signal that is generated by the PLL) with respect to phase and frequency. The function of the PLL can be explained from the block diagram of a simple PLL, as shown in Fig. 1.

The input signal $u_1(t)$ is compared with the reference signal $u_2(t)$ in the phase detector (PD). The output of the phase detector is zero as long as the input signal and the output signal is equal in phase and frequency. If the phase or frequency of the input signal changes, the output of the phase detector will deviate from zero. The error signal is passed through a low-pass filter (LF) and then to a voltage-controlled oscillator (VCO), which generates a reference signal (the output signal). If the error signal deviates from zero, the VCO will adjust the frequency of the reference signal so that the phase error becomes zero and the two signals are in phase. When the input signal is in phase with the reference signal, the PLL is in its locked state; hence the name phase locked.

Recent research related to PLLs has been from several research fields: general descriptions of PLLs [21], distributed generation applications [22], active power-line conditioner applications [23], servo controllers [24], as well as protection and control [25]–[27].

B. Description of a PLL that is Suitable for the Discrimination Between a Fault and a Switching Transient

A vector implementation, as shown in Fig. 2, of a PLL is described in this paragraph. Compared to the block diagram of Fig. 1, the error signal $e(t)$ corresponds to the output of the PD, whereas the proportional-integral (PI) regulator and the integrator corresponds to the loop filter and the voltage-controlled oscillator (VCO). The inputs to the PLL are the three phase-currents (I_a, I_b, and I_c), which are first transformed to $\alpha\beta$ quantities (I_α, I_β) using Clarke's transformation. Then, the $\alpha\beta$ quantities are projected onto a reference frame. Depending on the proximity of the $\alpha\beta$ quantities to the reference frame, an error signal is formed. This error signal is fed through a PI regulator

so that the error is controlled to zero. Once the error is zero, the input signals are in phase with the reference frame.

If it is assumed that the system is in steady state and that the power system is completely balanced, the phase currents can be written as

$$
\begin{aligned}
I_a &= I \cdot \sin(\omega t) \\
I_b &= I \cdot \sin\left(\omega t - 2 * \frac{\pi}{3}\right) \\
I_c &= I \cdot \sin\left(\omega t + 2 * \frac{\pi}{3}\right).
\end{aligned}
\tag{1}
$$

Then, the Clarke's components I_α and I_β equate to

$$
\begin{aligned}
I_\alpha &= \frac{(2 \cdot I_a - (I_b + I_c))}{3} = I\sin(\omega t) \\
I_\beta &= \frac{(I_b - I_c)}{\sqrt{3}} = -I\cos(\omega t).
\end{aligned}
\tag{2}
$$

Now, with reference to Fig. 2, the error signal is given by

$$
e(t) = I_\alpha \cdot \cos(\theta) + I_\beta \cdot \sin(\theta) = I\sin(\omega t - \theta).
\tag{3}
$$

Thus, the error is zero exactly when the output angle of the PLL is in phase with the current of phase a. When a transient occurs in the system, the error signal will deviate from zero. Depending on the characteristics of the transient, the deviation will have different magnitude and frequency. Since a fault is typically an ac fundamental power frequency character, the deviation will be different than for a switching transient that contains nonfundamental power frequency components. The behavior of the error signal of the PLL will also depend on the tuning of the PLL.

C. Tuning of the PLL

The PLL will be tuned to the power system frequency. PLLs have been used for many years in HVDC transmission in order to synchronize the firing of the thyristors to the phase angle of the connected ac system. It is thus a well-known procedure and it is advisable to use parameters from such an installation as a starting point for the tuning. Fine-tuning of the parameters can than be made by, for example, computer simulations or any other standard tuning method.

D. Fault Detection and Discrimination Using a PLL

The method that is used to detect a fault and discriminate the fault from a switching transient is described here. Two algorithms are executed in parallel. The first algorithm is based on the estimation of the magnitude of the current. If the estimated magnitude is higher than a preselected threshold, a flag is set. The second algorithm is as previously mentioned, monitoring the error signal of a PLL. If this error signal exceeds a preselected threshold, a second flag is set. If both flags are set, it is determined that a fault has occurred.

V. SIMULATION AND RESULT

In order to test the proposed method, a simple test system has been developed and implemented in an Electromagnetic Transients Program (PSCAD/EMTDC) [28].
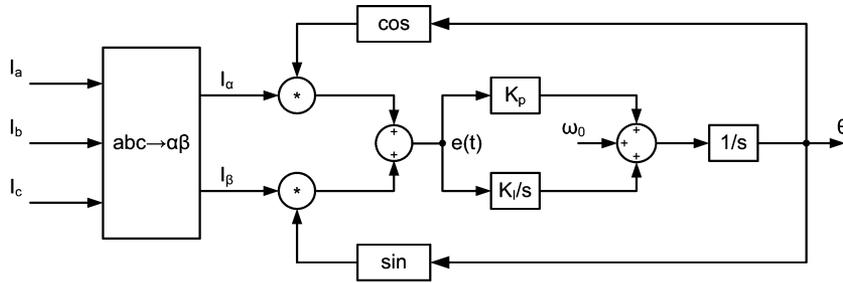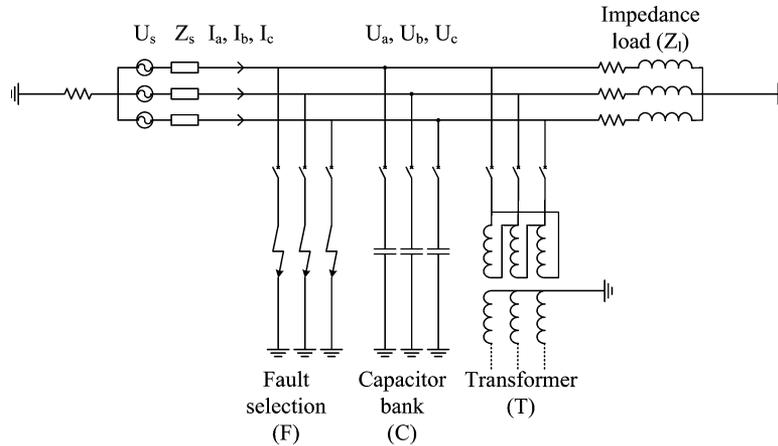
Fig. 2. PLL implementation.

Fig. 3. PSCAD/EMTDC test system.

The test system, as shown in Fig. 3, consists of an infinite source, an impedance load, a shunt capacitor (with an associated circuit breaker), a transformer (with an associated CB), and a fault selection arrangement. The data of the system are summarized as follows.

- The infinite source is modeled with a voltage source that is connected in series with an impedance. The supply voltage of the source has been chosen as $U_h = 12$ kV. The series impedance has been chosen so that the power system will have a short-circuit power of approximately $S_k = 831$ MVA ($R = 12.2$ mΩ, $L = 0.55$ mH). The supply frequency of the voltage source is selected to $f = 50$ Hz. A short-circuit power of $S_k = 831$ MVA will give a short-circuit current of approximately $I_k = 40$ kA.
- The impedance load is modeled by an impedance consisting of a resistor and an inductance. Their values are chosen so that the load current is approximately 630 A.
- The shunt capacitor is modeled by a capacitance of $C = 90.19\ \mu$F. The shunt capacitor gives a reactive power supply of 4.08 MVAr at nominal voltage. The shunt capacitor is connected to the power system by a CB which, at the start of the simulation, is open. The capacitor is uncharged at the start of the simulation.
- The transformer is modeled by a transformer model available in the master library of PSCAD/EMTDC. With this transformer model, it is possible to model inrush phenomena and magnetizing properties. The transformer is connected to the power system with a CB which, at the start of the simulation, is open. The transformer is

connected in delta on the primary side and in Y on the secondary side. The winding voltages of the transformer are 12 kV at the primary side and 240 V at the secondary side. The leakage reactance is 0.122 p.u. on a transformer rating of 10.2 MVA. The residual flux in the transformer is also modeled.

- The fault selection arrangement is implemented by using a component from the PSCAD master library. With this component, it is possible to simulate different fault resistances, whose phases participate in the fault and different fault inception angles. At the start of the simulation, no fault is applied.

A. Simulated Events

A large selection of shunt faults, capacitor energizations, and transformer energizations have been simulated. The faults were simulated as three-phase faults and phase-to-phase faults with low impedance. This selection was made because these types of faults are dimensioning for fault-current-limiting applications. Many distribution systems are earthed through an impedance, which limits the magnitude of fault currents due to single-phase earth faults. The capacitor and transformer energizations have been simulated by closing the associated CB. All events have been simulated to occur at various times with respect to the phase angle of the supply voltage (the phase angle of phase a has been selected as a reference). The instant when the event occur will determine some of the characteristics of the transient current such as, for example, the magnitude and possible dc offset.
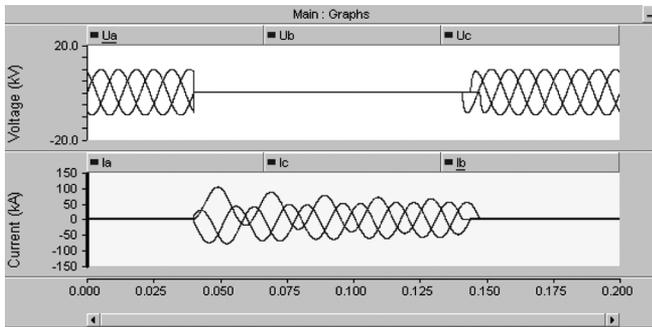
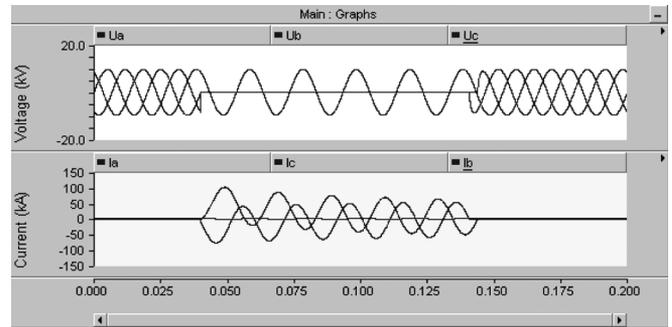Fig. 4.   Phase voltages and currents due to a three-phase fault.

Fig. 5.   Error signal due to a three-phase fault (in per unit).

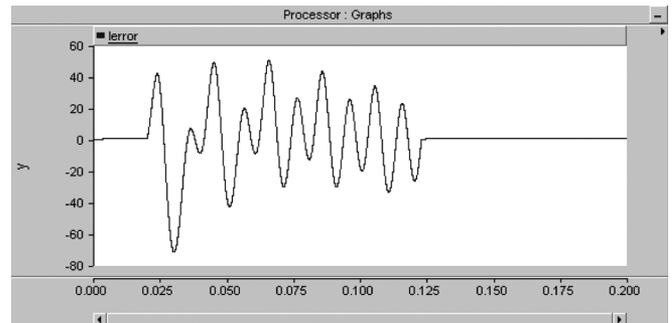Fig. 6.   Phase voltages and currents due to a phase-to-phase fault.

Fig. 7.   Error signal due to a phase-to-phase fault (in per unit).

Fig. 8.   Phase voltages and currents due to transformer energization.

Fig. 9.   Error signal due to transformer energization (in per unit).

B. Results

A large number of results are available as a result from the simulations. A few selected results are presented here. The figures of this subsection contain plots of power system signals—mainly voltages and currents—but also signals of the control system, such as the error signal from the PLL, which has been taken as a measure on how much the measured current deviates from the prefault load current.

1) Faults: This section contains plots of signals caused by shunt faults in the power system. Both three-phase and phase-to-phase faults have been analyzed. Typical phase voltages and currents due to a three-phase fault are plotted in Fig. 4. The error signal of the PLL for this fault is plotted in Fig. 5. As can be seen from that figure, the error signal deviates largely from zero (steady state) shortly after the fault. However, after the fault is cleared, the error signal returns to zero once the PLL has adjusted to the new conditions. Faults have been applied with different fault inception angles. The magnitude of the error signal of the PLL was well above 10 p.u. for all fault inception angles.

Typical phase voltages and phase currents due to a phase-to-phase fault are plotted in Fig. 6. The error signal of the PLL for this fault is plotted in Fig. 7. As can be seen from that figure, the error signal again deviates from zero shortly after the fault. Once the fault is cleared, the error signal returns to zero after a short transient period. Faults have been applied with different fault inception angles. The magnitude of the error signal of the PLL was well above 10 p.u. for all fault inception angles.

2) Transformer Energization: In this section, plots of signals (voltages, currents, and relevant parameters from the control system) caused by transformer energization in the power system are presented. Typical phase voltages and phase currents
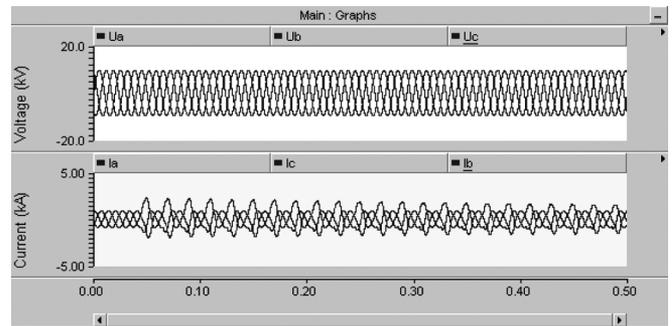
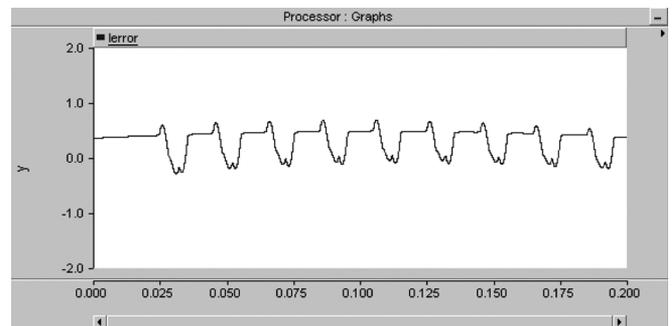due to a transformer energization are plotted in Fig. 8. The error signal of the PLL for this event is plotted in Fig. 9. As can be seen from that figure, the error signal deviates from zero shortly after the event has occurred but returns to steady state when the
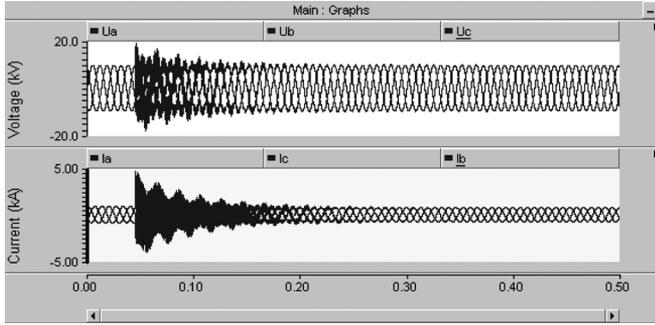
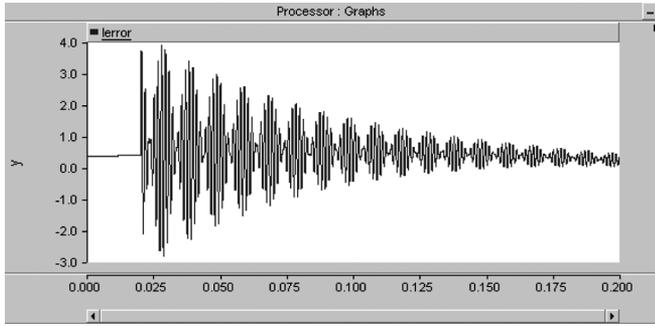Fig. 10.   Phase voltages and currents due to capacitor energization.

Fig. 11.   Error signal due to capacitor energization (in per unit.).

PLL has adapted to the new conditions. Different switching instants were investigated and the magnitude of the error signal was never above 2 p.u.

3) Capacitor Energization: In this section, plots of signals (voltages, currents, and relevant parameters from the control system) caused by capacitor energization in the power system are presented. Typical phase voltages and phase currents due to capacitor energization are plotted in Fig. 10. The error signal of the PLL for this event is plotted in Fig. 11. As can be seen from that figure, the error signal deviates from zero shortly after the event has occurred but returns to steady state when the PLL has adapted to the new conditions. Different switching instants were investigated and the magnitude of the error signal was never above 5 p.u.

C. Analysis of the Proposed Method

First, a threshold for the measured current magnitude is selected. In this example, the threshold is selected to three times the nominal current, (i.e., 2 kA). Second, a threshold for the error signal of the PLL is selected. In this example, the threshold is selected to 10 p.u. The first threshold is reached for all of the four transients studied in this section. However, the second threshold is only reached for the two transients that correspond to faults (i.e., the three-phase fault and the phase-to-phase fault). Thus, it can be concluded that the algorithm is able to discriminate between a fault and a switching transient. With a sampling rate of 64 samples/cycle (50 Hz), the first threshold is reached at the first sample following fault inception (i.e., after 0.3 ms). The second threshold is reached after approximately 2 ms. Thus, the fault detection time is approximately 2 ms.

Compared to a magnitude-based protection algorithm, all four transients would have been considered as faults since the first threshold was reached. In order to use a pure magnitude-based protection algorithm, the first threshold would have to be increased to, for example, 10 kA to provide a good margin between a fault and a switching transient. If the magnitude of the switching transients is higher, the threshold will have to be increased even more.

VI. CONCLUSION AND FUTURE WORK

In this paper, it has been demonstrated that a PLL can be used to determine whether a current transient is due to a fault in the system or due to a switching transient. Transformer and capacitor switching have been specifically studied due to the large occurrence of these switching transients in the power system. Simulations have been performed using a test system where faults and switching transients have been simulated. For all of these events, a large difference was observed in the error signal of the PLL when a fault or a switching transient was applied. This difference can be used to discriminate faults from switching transients.

The work presented in this paper is based on simulations and theoretical investigations. The focus has been on discrimination between switching transients and low impedance faults. For future work, high impedance faults must also be considered. Furthermore, the method could be tested in a real-time digital simulator with actual recordings of faults and switching transients and eventually implemented in a real protection system.

APPENDIX

RMS Value Calculation: The rms value of a current is estimated from measured current samples as

$$I_{\mathrm{rms}} = \sqrt{\frac{\sum_{k=0}^{n} i_k}{n}} \qquad (A.1)$$

where i_k denotes the measured current samples and n denotes the number of samples that are used for the rms calculation. Typically, n is selected so that the rms calculation is performed over one period of fundamental power system frequency.

FFT-Based Calculation: The peak value of a current is estimated from measured current samples in two steps. First, the orthogonal components I_c and I_s are calculated as

$$I_c = \frac{2}{K} \sum_{k=1}^{K} i_k \cos(k\theta) \qquad (A.2)$$

and

$$I_s = \frac{2}{K} \sum_{k=1}^{K} i_k \sin(k\theta). \qquad (A.3)$$

Finally, the estimated peak current is calculated as

$$I_p = \sqrt{I_c^2 + I_s^2}. \qquad (A.4)$$

Typically, the number K is selected so that the calculation covers one period of fundamental power system frequency.

LSQ-Based Calculation: The peak value of a current can be estimated from measured current samples by fitting the measured current samples to a signal model. Three measured current samples y_{-1}, y_0, y_1 can be fitted to the signal model

$$i(t) = I_c \cos \omega_0 t + I_s \sin \omega_0 t. \tag{A.5}$$

If it is assumed that the frequency in the system is known, the signal model contains two unknown parameters. The three measured current samples are fitted to the signal model by a least-square approach and I_c and I_s are calculated as

$$I_c = \frac{[i_1 \cos \theta + i_0 + i_{-1} \cos \theta]}{1 + 2 \cos^2 \theta} \tag{A.6}$$

and

$$I_s = \frac{[i_1 - i_{-1}]}{2 \sin \theta}. \tag{A.7}$$

Finally, the estimated peak current is calculated as

$$I_p = \sqrt{I_c^2 + I_s^2}. \tag{A.8}$$

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